**DCS Lab **

**Experiment - 9**

**Aim:** Counters and its applications

1: Implement a modulo 16 counter shown in Figure below. The counter have 4 bit parallel input I, control signals clock, clear, count enable and load. It has 4 bit output S and one bit output Terminal count. The relation between input and output ports are defined below.



In the simulations, show the regular count process for 20 cycles and also show the simulation for these cases

\_ CLR = 1, LOAD = 1, CNT =1, I = 0011

\_ CLR = 0, LOAD = 1, CNT =1, I = 0011

\_ CLR = 0, LOAD = 0, CNT =1, I = 0011



2: Using the modulo 16 counter designed in previous question as a component, design a 2 to 12 counter. Show at least 2 complete cycle of 2 to 12 counting in your simulation.